



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,996	01/20/2004	Scott L. Smith	72212	1657

27975 7590 08/25/2005

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER

BRINEY III, WALTER F

ART UNIT PAPER NUMBER

2646

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/760,996	Applicant(s) SMITH ET AL.	
	Examiner Walter F. Briney III	Art Unit 2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeshita et al. (US Patent 4,385,336).**

Claim 1 is limited to *a method of detecting a ground fault on a span-powered telecommunication wireline to which a remote telecommunication device is coupled and powered thereby*. Takeshita discloses a current supplying circuit with a shorted-to-ground fault detecting function. See Abstract. Generally depicted in figure 1, the current supplying circuit includes a battery (6) for supplying current on feed line (1) and a return for current upon feed line (2). Two resistor circuits (3) and (4) are connected in series with the feed lines, the current through the resistors detected by current detectors (8) and (9), respectively, and the detected currents through each resistor are compared by comparator (10) to detect a ground fault. See column 3, line 24, through column 4, line 8. With respect to the claim as recited, the current detector (8) and the current detector (9) perform functions corresponding to measuring first and second parameters representative of current flowing through a first and second portion of a wireline, respectively. The comparator (10) detects a difference between these parameters and

provides an output indicating a ground fault. Therefore, Takeshita anticipates all limitations of the claim.

Claim 2 is limited to *the method according to claim 1*, as covered by Takeshita.

Figure 3 depicts a more detailed view of one embodiment of figure 1. In particular, each of the resistors (3) and (4) comprise a resistor in series with the feed paths seen in figure 3. The resistors correspond to the recited first and second sense resistors. The recited first and second voltages correspond to either the voltages presented at nodes a and b of the differential amplifier (10) or the voltages across the base and emitter of transistors Q₆ and Q₇ or a combination thereof. In any case, the voltages are compared to each other due to the common emitter configuration of the differential amplifier (10). In response, an output SCN is generated, signaling the absence or presence of a ground fault. Therefore, Takeshita anticipates all limitations of the claim.

Claim 3 is limited to *the method according to claim 2*, as covered by Takeshita.

Still referring to figure 3, the sense resistor (3) is coupled to detector (8), which essentially mirrors a representative current through resistor R_{1A} to node "a." The current generated through circuit (8) is coupled to the differential amplifier (10). The amplifier allows output current to flow through resistors R₁₂; the current through the resistor leaks through the base to node "a" and through the collector to resistors R₉ and R₈. The base current combines with the mirror current to form the first voltage across resistor R₁₁. The collector current controls the current through transistor Q₈, which corresponds to a controlled current device. Therefore, Takeshita anticipates all limitations of the claim.

Claim 4 is limited to *the method according to claim 3*, as covered by Takeshita.

As seen in figure 3, the voltage across resistor R_{1B} is coupled to the inputs of a differential amplifier formed at least in part by the transistors Q_{12B} , Q_{13B} , Q_{1B} and Q_{0B} . The output voltage across resistor R_{0B} is passed to the base node "b" as the second voltage and is differentially combined with the voltage at node "a," which corresponds to the first voltage. Their difference indicates the presence or absence of a ground fault. Therefore, Takeshita anticipates all limitations of the claim.

Claims 5-8 are limited to *an apparatus for detecting a ground fault on a span-powered telecommunication wireline to which a remote telecommunication device is coupled and powered thereby*. The circuitry disclosed by Takeshita cited in the rejections of claims 1-4 corresponds to the first circuit section, second circuit section and differential circuit. In particular, the first circuit section includes resistor (3), the detector (8), transistor Q_6 and resistor R_{11} . These elements correspond to the first sense resistor, current mirror, differential amplifier and output resistor, respectively. The second circuit section includes the resistor (4), the detector (9) and transistors Q_{12B} , Q_{13B} and Q_{1B} . The resistor corresponds to the second sense resistor while the detector and transistors correspond to the differential amplifier coupled across said second sense resistor. The differential circuit includes all elements shown in amplifier block (10) including the controlled current device (Q_8) coupled in circuit with said current mirror. Therefore, Takeshita anticipates all limitations of the claims.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. (US Patent 4,385,336) in view of Phillips et al. (US Patent Application Publication 2004/0240665).**

Claims 9-12 are limited to *a method of detecting a ground fault on a span-powered telecommunication wireline within a plurality of span-powered wireline segments to respective ones of Digital Subscriber Line – Central Office Terminals (DSL-Cs) are coupled, so that a ground fault may be detected when power is delivered by the DSL-C over a respective wireline segment to a respective downstream functional Remote Terminal (RT).* While the steps described in claims 9-12 have already been shown to be fully anticipated by the disclosure of Takeshita, the shorted-to-ground fault detecting function of Takeshita is disclosed for general use only. There is no mention of a DSL-C within the disclosure of Takeshita, such that Takeshita necessarily fails to anticipate performing the steps at a DSL-C as recited.

Phillips teaches a power ramp-up in a line-powered network element system. In particular, a central office terminal (200) that supplies DSL service (i.e. a DSL-C) includes a method for power ramp-up where a ground fault detection is provisioned (step 416). See paragraph 43 and figure 4. As Phillips does not actually teach the manner in which a ground fault is detected, it follows that one of ordinary skill in the art

wishing to practice the invention of Phillips would be inherently motivated to use a prior art ground fault detection circuit. It would have been obvious to one of ordinary skill in the art to use the ground fault detection circuit as taught by Takeshita to implement the ground fault detection step (416) as taught by Phillips for the purpose of providing power ramp-up in a DSL-C


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB


SUHAN M
PRIMARY EXAMINER

Application/Control Number: 10/760,996
Art Unit: 2646

Page 7

8/19/05